Wideband Analog Front End IC

KAN1101

Brief Datasheet

Rev. 0.6.3b

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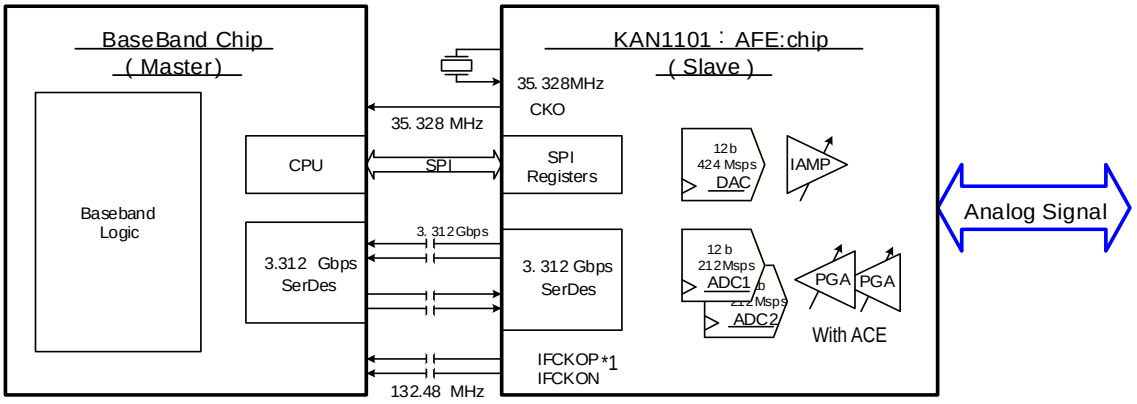
Abbreviations and Acronyms

ACE	Analog Channel Equalizer
AFE	Analog Front End
ASI	AFE Serial Interface 3.312Gbps Interface
CCITT	The previous name for ITU-T
CRC	Cyclic Redundancy Check
DAC	Digital to Analog Conversion
DSP	Digital Signal Processing
EMI	Electro Magnetic Interference
IAMP	Current Amplifier
JEDEC	Joint Electron Devices Engineering Council, an independent semiconductor engineering trade organization
JESD 204A	JEDEC standard, serial interface for converters
K28.5	Special code group name defined in 8B/10B transmission code
LVDS	Low Voltage Differential Signal
Msps	Mega Samples per Second
PCB	Printed Circuit Board
PGA	Programmable Gain Amplifier
PHY	Referred to the Digital portion of the Physical Layer
PLC	Power Line Communication
PLL	Phase Locked Loop
SerDes	Serializer and Deserializer
SPI	Serial Peripheral Interface
XAUI	A 10 Mbps Media Independent Interface between MAC and PHY layer, X refers to ten, AUI refer to Attachment Unit Interface.
OPM	Operational Mode

1. Features

- 65nm CMOS Wide Band Analog Front End IC
- 12mm x 12mm VQFN 88-pin 0.5mm pitch, or, 10mm x 10mm VQFN 88-pin 0.4mm pitch
- High speed sampling rate and low power consumption
- High resolution and wide frequency range
- Deep Sleep Mode Operation
- Up to 212 Msps data rate
- TxDAC Path
  - 12-bit 424Msps DAC
  - Pre-emphasis filter
  - Selectable low pass (0-95.4MHz or 0-100MHz) and high pass (116.6MHz-212MHz or 112-212MHz) mode 2x interpolator
  - Integrated 200mA line driver with 20dB gain control (bypass mode is supported)
- RxADC Path
  - 12-bit 424Msps by means of 2x 12-bit 212 Msps ADC with time interleaved manner
  - Low-noise PGA with ACE
  - Selectable low pass (0-95.4MHz or 0-100MHz) and high pass (116.6MHz-212MHz or 112-212MHz) mode /2 decimator
- Integrated low-jitter clock synthesizer (PLL)
- 3.312Gbps high speed serial interface as the digital interface (compatible with JESD204A)
- IFCKOP/N are the clean 132.48MHz clock output to be used as the reference clock for a baseband chip
- Integrated fine and accurate foreground calibration on TxDAC and RxADC path



Note :
1. The frequency of IFCKOP/N (differential reference clock) is 132.48MHz. SerDes in the baseband chip must support 25x for 3.312Gbps serial link (25x132.48MHz = 3.312GHz). 424Mbps(MHz) is actually 12x35.328MHz=423.936Mbps(MHz). 212Mbps(MHz) is actually 6x35.328MHz=211.968Mbps(MHz).
2. Figure 1 is the example for MCC internal use. 35.328MHz Xtal is connected to KAN1101 for generating internal clock and external clock on CKO. On G.fast application, 35.328MHz external clock is supposed to input both KAN1101 and BaseBand chip.

Figure 1 : Example of Applications

2. General Description

KAN1101 is among MCC's high-end integrated analog front end (AFE series) family of products. KAN1101 provides high performance, low power, and cost effective solution for home networking applications, wireless base station, and so on. KAN1101 integrates two analog-to-digital converters (ADC), programmable gain amplifier (PGA), analog channel equalizer (ACE), one digital-to-analog converters (DAC), one current amplifiers (IAMP), one clock synthesizer (LC-based), one 3.312Gbps serializer/deserializer (SerDes), serial peripheral interface (SPI), and digital signal processing units (DSP). KAN1101 is available in 65nm CMOS technology.

Figure 2 shows the AFE overall block diagram. PGA has the function of ACE to compensate higher frequency signals which are largely attenuated over long distance which usually results in lower SNR on receiver side. DAC is 12-bit 424Msps. Two ADCs are identical and operating at 12-bit 212Msps to achieve 12-bit 424 Msps by means of time interleaved manner. The 12-bit sampling data is transferred between the baseband (Digital PHY) chip and KAN1101 via the SerDes at 3.312Gbps serial bit stream. A simple protocol to convert the 12-bit to the serial bit stream and vice versa is defined as the ASI (AFE Serial Interface), which is compatible with JESD 204A (JEDEC standard, serial interface for converters). The ASI defines framing, scrambling, 8B/10B coding, establishing and maintaining the 3.312Gbps link. The serial interface, as adopted by many similar standards provides a number of advantages which include simpler PCB design, reduced EMI, lower pin counts, etc. Tx can provide a full scale current in the range of 4mA to 200mA by IAMP. IAMP can be bypassed. Note that either IAMP enabled or bypassed can be chosen at a time (these are exclusive). The PGA gain can be configured from -18 dB to 24 dB. The clock synthesizer is an LC-VCO based PLL technology with low jitter employing the 35.328MHz Xtal input as its reference clock. The sampling clocks and the differential reference clock to the SerDes are derived from the PLLs and are carefully routed to maintain the signal quality and integrity. The differential reference clock is also output on IFCKOP/N through LVDS driver. The frequency of the differential clock is 132.48MHz. It shall be used as the reference clock of the SerDes in a baseband chip for ASI.

The digital signal processing units realize FIR filters, such as pre-emphasis, interpolator, decimator, and calibrations for DAC, PGA, and ADCs. The DSP units are among the important blocks within KAN1101 to maintain the utmost performance. KAN1101 provides the optimum control for power consumption within the device by switching on/off each component's operation. The target system can be optimized by configuring KAN1101 via the three or four wire SPI Interface.

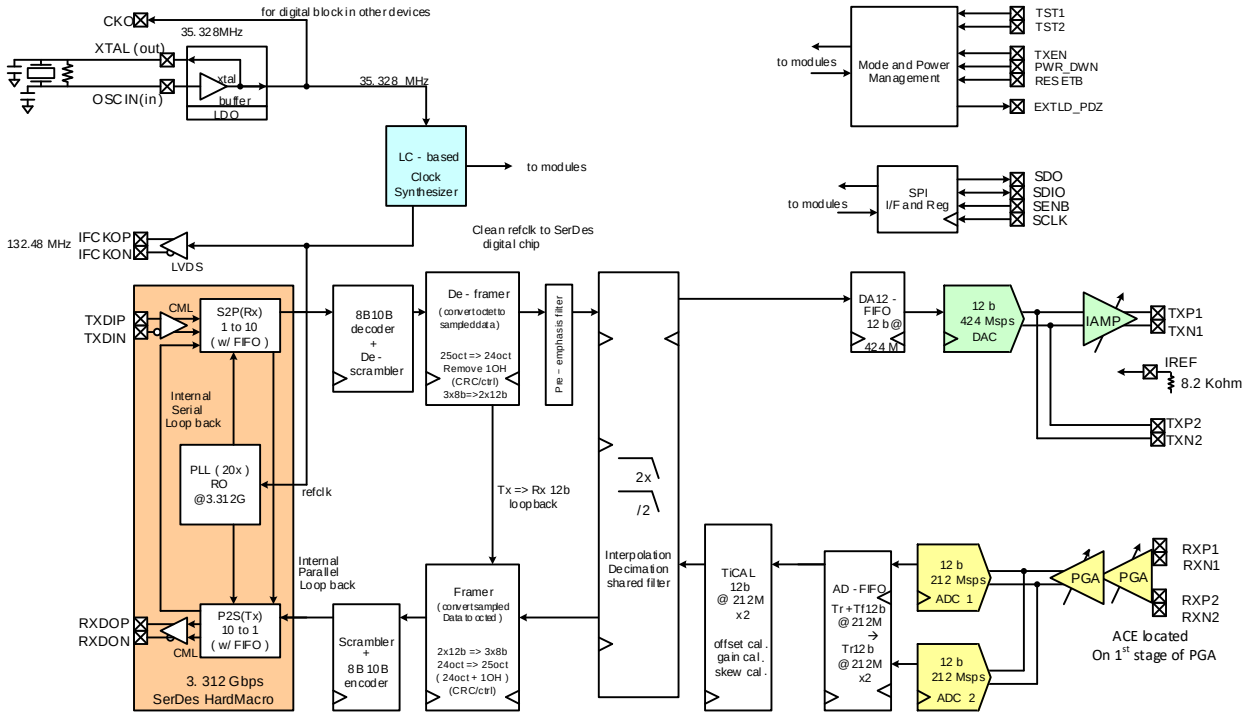


Figure 2 : Block Diagram

3. Electrical Characteristic

3.1. Absolute Maximum Rating

Table 1 : Absolute Maximum Rating

Parameter Description	Min	Typ	Max	Unit	Note
2.5V power supply	-0.3	-	4.0	V	-
1.2V power supply	-0.3	-	1.6	V	-
Voltage on LVTTL Signal	-0.3	-	IOVDD + 0.3	V	-
Voltage on LVDS Signal	-0.3	-	SDS_A25_VD + 0.3	V	-
Voltage on analog signal	-0.3	-	(analog 2.5V) + 0.3	V	-
Voltage on CML signal	-0.3		SDS_A12_VD(1.2V) + 0.3	V	
Storage Temperature	-55	-	125	°C	-

3.2. Recommended Operating Condition

Table 2 : Recommended Operating Condition

Parameter Description	Symbol	Min	Typ	Max	Unit	Note
1.2V analog power supply	ADC_A12_VD ADC_D12_VD ADC_AVDDREF DAC_A12_VD BIAS_A12_VD SDS_A12_VD (PLL_EXT_CAP1/2)	1.14	1.2	1.26	V	1
2.5V analog power supply	PLLSDS_A25_VD SDS_A25_VD LVDS_A25_VD PLL_A25_VD DAC_A25_VD PGA_A25_VD BIAS_A25_VD ANALPBK_A25_VD	2.375	2.5	2.625	V	1
1.2V Digital Power Supply	VDD	1.14	1.2	1.26	V	1
2.5V Digital Power Supply	IOVDD	2.375	2.5	2.625	V	1
IAMP output compliance voltage	OCV_IAMP	0.7		5	V	
DAC output compliance voltage	OCV_DAC	0		0.5	V	
Noise on Analog Power Supply within 10 MHz	PSnoise	-	-	6	mV	
External Resistor on IREF	REXT_IREF	-	8.2	-	Kohm	-
External Resistor on SDS_REXT	REXT_SDS	-	3	-	Kohm	-
External Capacitance on OSCIN and XTAL	CEXT_OSC	The value is determined by X-tal.			pF	5
External Resistor between OSCIN and XTAL	REXT_OSC	-	1	-	Mohm	-
Ambient Temperature	Ta	-40	25	85	°C	-
Reference Clock Frequency	Fref	35.328MHz			-	-
Reference Clock Phase Jitter within10 MHz	Refj	-	-	0.35	ps	-
AFE Serial Interface Data Rate	ASIDrate	3.312Gbps			-	-
Receiver Jitter Tolerance	JitTol	0.65	-	-	UI	2
Transmit Jitter at 3.312Gbps	JitGen	-	-	0.55	UI	3
IFCKOP/N Clock Output Frequency	Fifcko	132.48MHz			-	-
IFCKOP/N Clock Output RMS Jitter	RMSJit_Ifcko	-	-	2	ps	-
IFCKOP/N Clock Output Duty Cycle	DCY_Ifcko	40	-	60	%	-
CKO Clock Output Frequency	Fcko	35.328MHz			-	-
CKO Clock Output Cycle-to-cycle Jitter	C2CJit_cko	-	-	190	ps	4
CKO Clock Output Duty Cycle	DCY_cko	35	-	65	%	-

Note:

1. Voltage values are tentative.
2. 0.65UI consists of 0.55UI Tj (incl. minimum of 0.37UI Dj) + 0.1UI Sj as specified XAUI standard
3. 0.55UI is as far-end specification
4. The frequency of IFCKOP/N (differential reference clock) is 132.48MHz. SerDes in the baseband chip must support 25x

for 3.312Gbps serial link (25x132.48MHz = 3.312GHz)
5. CEXT_OSC = 2*(CL - Cz), CL is X-tal's load capacitance, Cz is stray capacitance.

3.3. Power Dissipation (To be updated)

Table 3 : Power Dissipation

Parameter	Power Supply	Temp	Min	Typ	Max	Unit
Power Dissipation in Tx mode	Analog 1.2V	25C	-	20	-	mW
	Analog 2.5V	25C	-	605	-	mW
	Digital 1.2V	25C	-	210	-	mW
	Digital 2.5V	25C	-	19	-	mW
	Total	25C	-	853	-	mW
Power Dissipation in Rx mode	Analog 1.2V	25C	-	133	-	mW
	Analog 2.5V	25C	-	116	-	mW
	Digital 1.2V	25C	-	224	-	mW
	Digital 2.5V	25C	-	19	-	mW
	Total	25C	-	491	-	mW

Note:
1. Estimated value by simulation w/ ideal power supply.
2. Internal LDOs are not active (bypass mode).

3.4. TxDAC Specifications (To be updated)

Table 4 : TxDAC Specifications

Parameter	Temp	Min	Typ	Max	Unit	Note
TX1 (DAC + IAMP) DC CHARACTERISTICS						
Resolution	Full	-	12	-	Bits	
Update rate	Full	-	-	424	MSPS	1
Full-Scale Output Current (IFS) at Min and Max gain setting	25C	4	-	200	mA	2
Gain Error	Full		TBD		dB	
Offset Error	Full		TBD		% of FS	
Voltage Compliance Range	Full	0.7		5.0	V	
TX1 (DAC + IAMP) GAIN CONTROL CHARACTERISTICS						
Minimum Gain	25C	-	-14	-	dB	3
Maximum Gain	25C	-	20	-	dB	3

Parameter	Temp	Min	Typ	Max	Unit	Note
Gain Step Size	25C	-	TBD	-	dB	3
Gain Step Accuracy	Full		Monotonic		dB	3
Gain Range Error	Full		TBD		dB	3
TX1 (DAC + IAMP) AC CHARACTERISTICS 424Msps, IFS=178mA, MTPR						
@ 10MHz	25C	-	52.9	-	dB	4
@ 50MHz	25C	-	51.4	-	dB	4
@ 95MHz	25C	-	50.1	-	dB	4
IAMP Output Capacitance	Full		TBD		Ω||pF	
DAC (IAMP bypassed) DC CHARACTERISTICS						
Resolution	Full	-	12	-	Bits	
Update rate	Full	-	-	424	MSPS	1
Full-Scale Output Current (IFS) at Min and Max gain setting	25C	4	10	20	mA	5
Absolute Gain Error	25C	-	TBD	-	dB	5
Offset Error	25C	-	TBD	-	% of FS	5
Voltage Compliance Range	25C	0	-	0.5	V	5
DAC (IAMP bypassed) GAIN CONTROL CHARACTERISTICS						
Minimum Gain	25C	-	-14	-	dB	3
Maximum Gain	25C	-	0	-	dB	3
Gain Step Size	25C	-	TBD	-	dB	3
Gain Step Accuracy	Full		Monotonic		dB	3
Gain Range Error	Full		TBD		dB	3
DAC (IAMP bypassed) AC CHARACTERISTICS 424Msps, IFS=20mA, MTPR						
@ 10MHz	25C	-	54.0	-	dB	4
@ 50MHz	25C	-	52.4	-	dB	4
@ 95MHz	25C	-	52.0	-	dB	4
DAC Output Capacitance	25C		100||6		Ω||pF	5
TX DIGITAL FILTER CHARACTERISTICS						
pass band edge (-0.2dB BW)	Full		Refer to Table 17		fout/fDAC	6
Rejection ratio	Full		Refer to Table 17		dB	6
TX Path Latency	Full		Refer to		ns	6

Note :

1. 424Mbps(MHz) is actually 12x35.328MHz=423.936Mbps(MHz).
2. Ideal values set in Tx gain range.
3. Reference current in dB unit is 20mA. For example, 200mA is equal to 20*log (200mA/20mA) = 20dB
4. Estimated value by simulation w/ ideal condition of power supply, clock and transmission line.
5. Not silicon proven values, from DAC IP's specification
6. Whole gain setting in Tx active mode

3.5. RxADC Specifications (To be updated)

Table 5 : RxADC Specifications

Parameter	Temp	Min	Typ	Max	Unit	Note
RX INPUT CHARACTERISTCS (Legacy mode)						
Input Voltage Span						
RxPGA Gain = -16dB	25C	-	6.3	-	Vppd	1
RxPGA Gain = 24dB	25C	-	62.5	-	mVppd	1
Maximum Differential Input Voltage Swing	Full	-	-	7	Vppd	2
Differential Input Impedance	25C		Refer to Figure 28		Ω||pF	
Input Voltage Noise Density						
RxPGA Gain = 0dB	Full		TBD		nV/rtHz	
RxPGA Gain = 24dB	Full		TBD		nV/rtHz	
RX PGA CHARACTERISTICS (Legacy mode)						
Minimum Gain	25C	-	-18	-	dB	3
Maximum Gain	25C	-	24	-	dB	3
Gain Step Size	25C	-	1	-	dB	3
Gain Step Accuracy	Full		Monotonic		dB	4
Gain Range Error	Full		TBD		dB	
RX PGA CHARACTERISTICS (ACE mode)						
Minimum Gain	25C		Refer to Figure 24 and Figure 25		dB	
Maximum Gain	25C		Refer to Figure 24 and Figure 25		dB	
Gain Step Size	25C		Refer to Figure 24 and Figure 25		dB	
Gain Step Accuracy	Full		Monotonic		dB	4
Gain Range Error	Full		TBD		dB	
RX ADC CHARACATERISTICS						
Resolution	NA	-	12	-	Bits	
Update Rate	Full	-	-	212	MSPS	5
RX AC CHARACTERISTICS						
424Msps, RxPGA=0dB, MTPR						
@ 10MHz	25C	-	49.7	-	dB	6
@ 50MHz	25C	-	49.6	-	dB	6
@ 95MHz	25C	-	49.3	-	dB	6
424Msps, RxPGA=24dB, MTPR						
@ 10MHz	25C	-	40.0	-	dB	6
@ 50MHz	25C	-	39.6	-	dB	6
@ 95MHz	25C	-	40.0	-	dB	6
RX DIGITAL FILTER CHARACTERISTICS						
pass band edge (-0.2dB BW)	Full		Refer to Table 17		fout/fDAC	7
Rejection ration	Full		Refer to Table 17		dB	7
RX Path Latency	Full		Refer to Table 35		ns	7

Note :

1. Theoretical value
2. As absolute maximum rating.
3. These value are ideal in Rx gain setting range.
4. The values of min/max are for Legacy Mode. Gain value varies at frequency on ACE ON/OFF mode.
5. 212Mbps(MHz) is actually 6x35.328MHz=211.968Mbps(MHz).
6. Estimated value by simulation w/ ideal condition of power supply, clock and transmission line.
7. By means of time-interleave manner, Rx max sampling rate becomes 424Msps

Revision History

Document Revision	Revision Date	Summary of Change	Section/Page Changed
0.6.3b	Sep 4, 2017	Initial Release	-

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