

KL5BPLC200WMP

HD-PLC Data Processing IC

Databrief

Rev. 0.7.2

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1 Product overview

1.1 Function Overview

The KL5BPLC200WMP is an HD-PLC LSI designed to connect a wide range of home network devices in a flexible manner using existing residential electrical wiring. Its capabilities include transmission of high-definition video and other broadband content. HD-PLC is the name of a high definition power line communication system put forth by Panasonic.

Thanks to compatibility with the ubiquitous Ethernet standard, the KL5BPLC200WMP can be easily connected to network-enabled products such as broadband networks, televisions, and computers anywhere there is an electrical outlet simply by supporting the Internet protocol (IP), which already enjoys widespread use.

The KL5BPLC200WMP incorporates a 32-bit RISC processor and provides a single-chip implementation of high-performance wavelet conversion OFDM functionality, MAC processing functionality with high-quality QoS support, and HD-PLC/Ethernet bridge functionality.

QoS functionality can be used to guarantee a fixed communication speed for a variety of communications ranging from data transmission and reception to video streaming and IP telephony.

The KL5BPLC200WMP also has highly integrated analog front-end chip so that no other analog front-end IC for PLC is necessary. An on-chip PLL multiplier and synthesizer provide all the required clock signals from a single crystal or clock source.

Following are the features of KL5BPLC200WMP.

- Single chip solution for HD-PLC application.
- Network construction and optimization, advanced network diagnostics and management.
- HD-PLC network bridge function compatible with Ethernet address system.
- Ensuring the security and easy connectivity by data encryption using AES.
- High-speed communications up to 432 carriers within 2-28MHz band(Maximum PHY Rate: 240Mbps without notch)
- Determine the optimal rate according to the power line channel characteristics with the multilevel modulation for each sub-carrier.
- Optional sub-carriers masking function to be adapted to individual country's regulations.
- Level-up function to achieve maximum speed under individual country's regulations.
- Error correction and selective transmission retry to achieve efficient frame transfer.
- Backward compatible with existing 1st, 2nd HD-PLC systems.
- IEEE1901 compliant(Wavelet MAC/PHY, ISP)

1.2 Block Diagram

Figure- 1 shows a block diagram of the KL5BPLC200WMP.

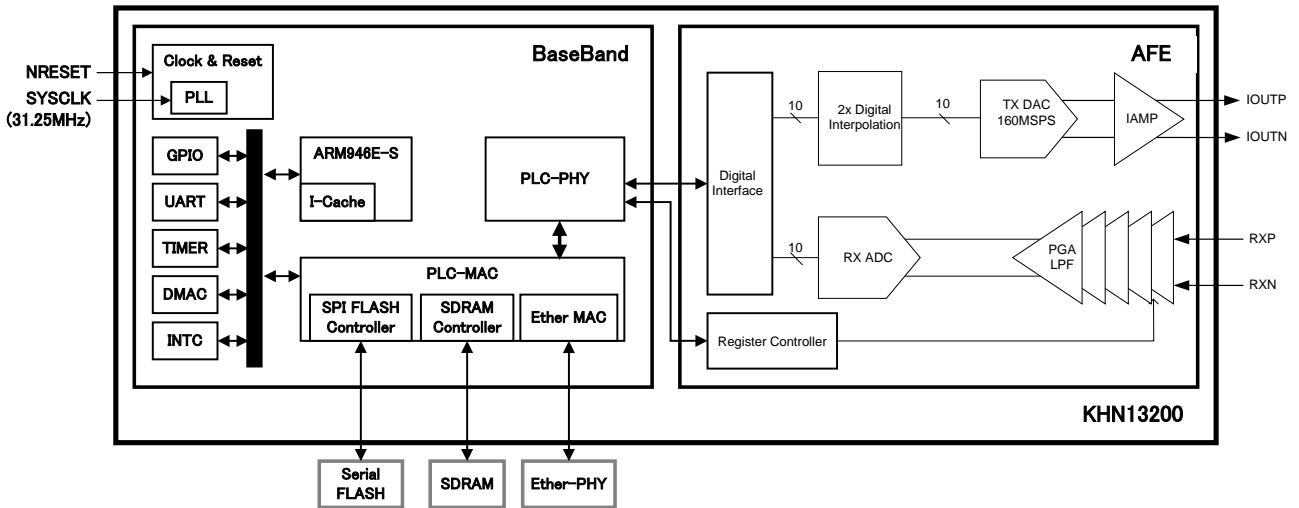


Figure- 1 KL5BPLC200WMP Block Diagram

2 Pins

2.1 Pin Assignments

Pin	Signal	Pin	Signal	Pin	Signal
1	GPIO6	108	AVSS		
2	GPIO7	107	AVSS		
3	GPIO8	106	AVSS		
4	KME_TEST	105	PLLDVSS		
5	IOVDDW	104	PLLAVSS		
6	GPIO9	103	PLLDVDD		
7	GPIO10	102	PLLAVDD		
8	EXTINT/GPIO12	101	IOVDDW		
9	MOSI	100	CVDD		
10	SCK	99	AVSS		
11	MISO	98	A33VDD		
12	CS	97	IREF		
13	SDDQ0	96	SERIAL_TXD		
14	SDDQ1	95	A12VDD		
15	SDDQ2	94	SERIAL_RXD		
16	SDDQ3	93	A33VDD		
17	SDDQ4	92	IOVDDW		
18	SDDQ5	91	CVDD		
19	SDDQ6	90	AVSS		
20	CVDD	89	RXP		
21	IOVDDW	88	RXN		
22	SDDQ7	87	AVSS		
23	SDDQM0	86	A33VDD		
24	SDWE	85	PHYCLOCK		
25	SDCAS	84	AVSS		
26	SDRAS	83	A12VDD		
27	IOVDDW	82	A12VDD		
28	BA0	81	TXEN		
29	BA1	80	TXD3		
30	CVDD	79	TXD2		
31	IOVDDW	78	TXD1		
32	SDA10	77	TXD0		
33	SDA0	76	IOVDDW		
34	SDA1	75	CVDD		
35	SDA3	74	AVSS		
36	SDA2	73	TXC		
37	SDDQ15	72	RXER		
38	SDDQ14				
39	CVDD				
40	IOVDDW				
41	SDDQ13				
42	SDDQ12				
43	SDDQ11				
44	IOVDDW				
45	IOVSS				
46	AFE_CLKO				
47	SDDQ10				
48	SDDQ9				
49	SDDQ8				
50	SDDQM1				
51	SDA12				
52	SDCLK				
53	IOVDDW				
54	SDA11				
55	SDA9				
56	SDA8				
57	IOVDDW				
58	SDA7				
59	SDA6				
60	SDA5				
61	SDA4				
62	IOVDDW				
63	RXD0				
64	RXD1				
65	RXD2				
66	RXD3				
67	ZEROX				
68	IOVDDW				
69	NRESET				
70	RXDV				
71	RXC				
72	RXER				
144	GPIO5				
143	GPIO4				
142	GPIO3				
141	IOVDDW				
140	GPIO2				
139	GPIO1				
138	GPIO0				
137	CLKOUT2				
136	DI2VDD				
135	DVSS				
134	OSG33VDD				
133	IOVDDW				
132	CVDD				
131	OSCI				
130	XTAL				
129	IOVDDW				
128	OSCVSS				
127	CONFIG				
126	MODE				
125	AFE_RXEN				
124	LINK				
123	IOUTP				
122	IOUTN				
121	MDIO				
120	CVDD				
119	A12VDD				
118	REVISION5				
117	REVISION4				
116	REVISION3				
115	REVISION2				
114	COL				
113	REVISION1				
112	REVISION0				
111	MDC				
110	GRS				
109	SYSCLK				

Figure- 2 Pin Assignment

3 Operating Conditions

3.1 Absolute Maximum Ratings

Table- 1 shows absolute maximum ratings.

Table- 1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
External supply IO voltage	V_{IOVDDW}	-0.3 to 4.0	V
External supply Analog voltage	V_{A33VDD}	-0.3 to 4.0	V
External supply Analog voltage	$V_{OSC33VDD}$	-0.3 to 4.0	V
Internal supply voltage for BaseBand	V_{CVDD}	-0.3 to 1.32	V
Internal supply voltage for AFE (Analog Part)	V_{A12VDD}	-0.3 to 1.6	V
Internal supply voltage for AFE (Digital Part)	V_{D12VDD}	-0.3 to 1.6	V
Input pin voltage	V_I	-0.3 to $V_{IOVDDW} + 0.3$	V
Analog Input/Output Voltage RXP,RXN,IREF IOUTP, IOUTN OSCIN, XTAL	V_{A1} V_{A2} V_{A3}	-0.3 to $V_{A33VDD} + 0.3$ -0.3 to 6.0 -0.3 to $V_{OSC33VDD} + 0.3$	V V V
Output current (2mA)	I_O	-5.2/+15.9	mA
Output current (4mA)	I_O	-10.6/+31.7	mA
Output current (8mA)	I_O	-21.2/+63.4	mA
Power dissipation	P_D	700	mW
Storage temperature	T_{stg}	-55 to 125	°C

Note:

- The absolute maximum ratings are the limit values beyond which the IC may be damaged. Operation is not guaranteed under these conditions.
- Directly connect all VDD pins to external power supplies and ground all VSS pins.
- Ensure that the junction temperature (T_j) is 125°C or less during use.

3.2 Recommended Operating Conditions

Table- 2 shows recommended operating conditions.

Table- 2 Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
External supply voltage	V_{IOVDDW} V_{A33VDD} $V_{OSC33VDD}$	---	3.1	3.3	3.5	V
Internal supply voltage	V_{CVDD} V_{A12VDD} V_{D12VDD}	---	1.1	1.2	1.3	V
Operating package surface temperature	T_C	$T_j = 125^\circ\text{C}$	-40	---	85	°C

4 Package

Figure- 3 shows the package outline of KL5BPLC200WMP (Exposed TQFP-144 pins).

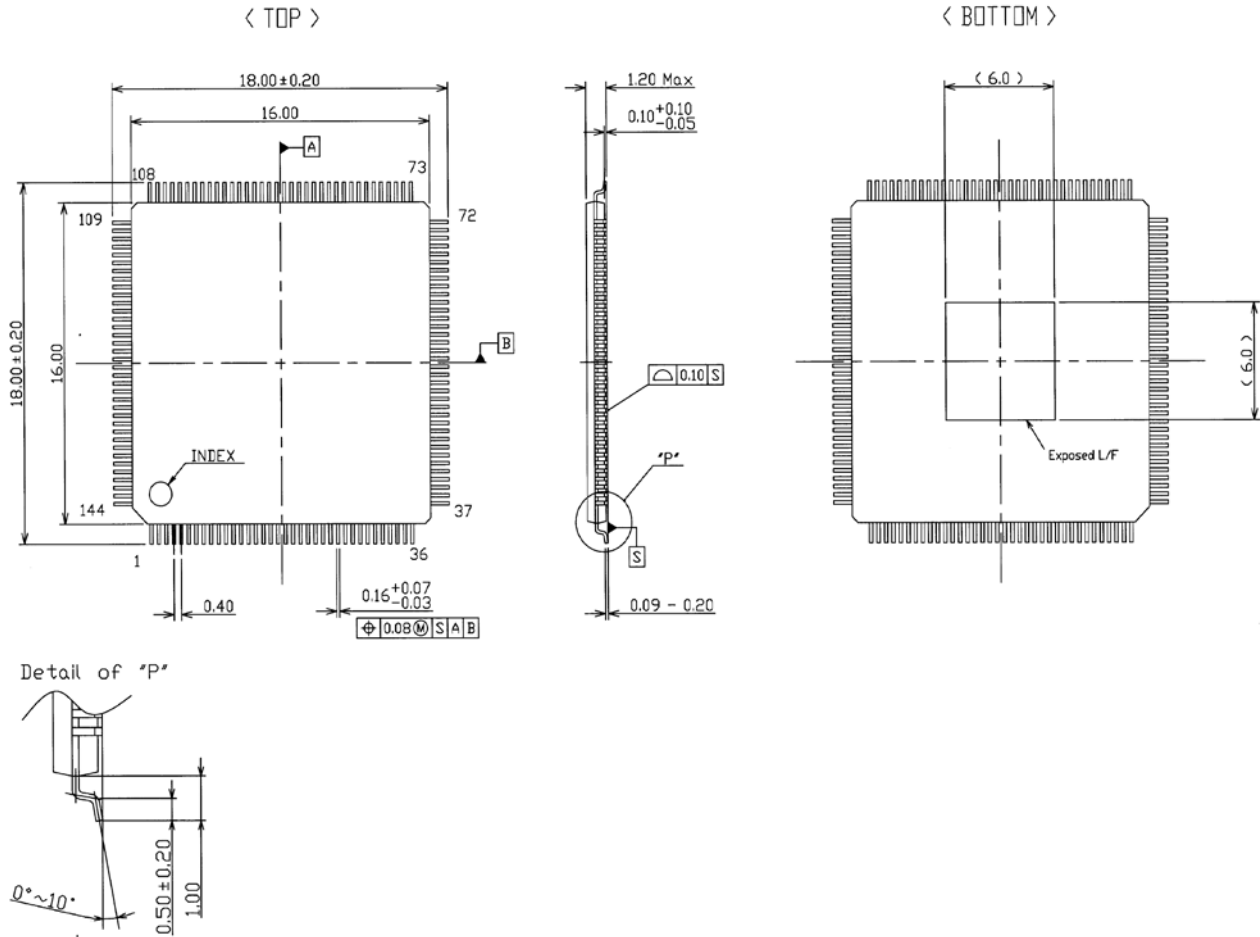


Figure- 3 KL5BPLC200WMP package outline (Exposed TQFP-144 pins)

5 Ordering Information

Part Number: KL5BPLC200WMP

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